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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,076	01/31/2002	Masato Kobayashi	FUJH 19.387	2478

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EXAMINER
CHANG, EDITH M

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,076	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Edith M. Chang	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on August 10, 2005 have been fully considered but they are not persuasive.

Argument: Applicants argues that the present invention controls a read clock based on the interval from an address designated by the read unit to an address designated by the write unit. In contrast, Murakami controls a read clock based on a stuff rate.

Response: In Fig.11 ('074), Murakami teaches an address control circuit 204 receiving clock signals from the phase locked loop circuit 6 to control the read address generating circuit 203 to properly space (an interval) the write address 253 and read address 256 (column 13, lines 57-60) and to control the read address generating circuit 203 at the initial setting (column 13, lines 60-62). As a result, the write address 253 and the read address 256 are properly spaced from each other. Hence, Murakami teaches the read address generating circuit 203 to adjust a cycle of the read clock signal based on the interval (space) of the write address 253 and read address 256.

Argument: Applicants argues that Murakami does not disclose the prevention of the overflow or underflow of the memory.

Response: The limitations of preventing overflow or underflow are not recited in the claims.

Claim Objections

2. Claims 7 and 9 are objected to because of the following informalities:

Claim 7, line 8: "a variable frequency divider of an output clock signal" should be "a frequency divider of an input clock signal"; line 9: "said frequency divider" should be "a variable frequency divider".

Claim 9 is dependent on the objected claim 7.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (Admission) in view of Murakami (US 6,658,074 B1).

Regarding to **claim 1**, In Fig.7 of the current application, the admitted prior art teaches all subject matter: a memory unit (102); a write unit (106); a write controller (104); a read clock signal generator (120); and a read unit (113) as recited in the claim, except a read clock signal regulator. However, Murakami teaches a technique for reproducing clock signal at a receiver in a pulse stuffed synchronization system (column 1 lines 8-10 & 24-33). In FIG.4, Murakami teaches an embodiment of the technique with

stuff rate measuring circuits 3 & 13, a control circuit 14 providing a divide ratio to the variable frequency dividing circuit 5 which in term provides a control signal 57 (654 Fig. 13) to the phase locked loop circuit 6 (detail shown in Fig. 13, as the read clock generator, column 6 lines 19-27) to provide the read clock signal 58 (255 Fig. 11, detail diagram of a storage circuit 2 with an address control circuit 204 shows a prescribed order direction) to adjust the read address (column 13, lines 57-60) via read address generating circuit 203 (Fig.11) of the storage circuit 2, wherein the STS-1 is the high order group signal and the DS3 is the lower order group signal.

At the time of the invention was make, it would have been obvious to a one of ordinary skill in the art to have the stuff rate measuring circuits, control circuit and variable frequency dividing circuit taught by Murakami coupled to the destuflfing control circuit 104 and the phase locked-loop circuit 120 of the admitted prior art (Fig.7) to provide a clock signal reproducing circuit for the benefits of having an efficient circuit with small circuit size and frequency division ration to reproduce a lower order group signal form a higher order group signal (column 5 line 60-column 6 line 7).

Regarding to **claim 2**, Murakami teaches a plurality of stuffing enable periods q (column 14 lines 11-21) to adjust clock timings.

Regarding to **claim 3**, in Fig.4, Murakami teaches the control circuit 14, the variable frequency dividing circuit 5, and the phase locked loop circuit 6 adjust the cycle of the read clock signal 58, wherein the PLL circuit 6 locks the cycle if the cycle is the DS3 (a predetermined interval), lengthen the cycle if it is shorter than the DS3, or

shorten if it is longer than the DS3. It is the PLL feature/function to adjust/lock the clock and is well known in the art.

Regarding to **claims 4** & **5**, in Fig.4, Murakami teaches the read clock signal 58 adjusted based on two stuff rates, the first is generated by the stuff rate measuring circuit 3 to detect the positive/zero/negative stuffing in the STS-1 signal (column 16 lines 23-26), and the second is generated by the stuff rate measuring circuit 13 to detect the positive stuffing in the overhead of STS-1 SPE and the unwanted bits in the overhead of STS-1 SPE signal are deleted (column 16 lines 33-40) wherein the unwanted bits in the overhead of STS-1 SPE apart substantially equal time intervals (as defined in Fig. 17 & 18).

Allowable Subject Matter

5. Claims 6, 8, and 10-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 7 and 9 would be allowable if rewritten to overcome the objection(s) set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest, alone or in a combination, among other things, at least a receiver apparatus for receiving digital data in which stuff data

have been inserted by stuffing synchronization as a whole, the combination of elements and features, which includes a read clock signal regulator increments or decrements a division ratio of a variable frequency divider by 1 to adjust the cycle of the read clock signal, wherein the division ration has the same numerical values as the number of bits held in each memory cells; or a frequency divider with a division ration of N for dividing an input clock signal, another frequency divider with a division ration of M for dividing an output signal of the VCO, wherein N:M equals to a ration between data volume of the overhead part and the payload part of a frame, and the read clock signal regulator increments or decrements the division ration of the another frequency divider by 1 to adjust the cycle of the read clock signal as cited in the claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ranganath et al. (US 6,836,854) describes a desynchronizer with a module for providing uniformly gapped data signal to a PLL module in FIG.1, the desynchronizer includes a gap regulator, pointer leak logic (FIG.4) adjusting the read point by control the reader counter based on the S-bin Control and the periodic interval.

Choi (US 4,764,941) describes a digital frame synchronizer in FIG.5 by positive or negative stuffing (column 1, lines 20-30). The frame synchronizer comprises a read counter (503) controlled by the stuffing decision (506) based on an interval of the latched write address and the latched read address (column 3, lines 20-26).

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M. Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay K. Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
November 21, 2005

KHAI TRAN
PRIMARY EXAMINER